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Sir:

Transmitted herewith for filing is the patent application of

Inventors: Joshua I. Pine

For: System for Improving the Dynamic Range of Solid-state
Imaging Devices

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Enclosed are:

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☒ an executed oath or declaration, with power of attorney.
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☐ ___ sheet(s) of informal drawing(s).
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Fee Calculation For Claims As Filed

a) Basic Fee									\$	710.00
b) Independent Claims	4	-	3	=	1	X	\$80.00	=	\$	80.00
c) Total Claims	35	-	20	=	15	X	\$18.00	=	\$	270.00
d) Fee for Multiple Claims					0	X	\$260.00	=	\$	0.00
Total Filing Fee									\$	1,060.00

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SYSTEM FOR IMPROVING THE DYNAMIC RANGE OF SOLID-STATE IMAGING DEVICES

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BACKGROUND OF THE INVENTION

1. Technical Field.

This invention relates to a solid-state imaging device with substantially improved dynamic range.

2. Related Art.

Solid-state imaging devices (also referred to as image devices or imagers) have broad applications in many areas including commercial, consumer, industrial, medical, defense and scientific fields. Solid-state imaging devices convert a received image from an object into a signal indicative of the received image. Solid-state imaging devices are fabricated from semiconductor materials (such as silicon or gallium arsenide) and include photosensitive imaging arrays (photosensors) of light detecting picture elements, or pixels, (also known as photodetectors) interconnected to generate analog signals representative of the received image. Examples of solid-state imaging devices include charge coupled devices (CCD), photodiode arrays, charge injection devices (CID), hybrid focal plane arrays and complementary metal oxide semiconductor (CMOS) imaging devices.

Photosensors of the solid-state imaging devices are typically formed in an array structure, with rows and columns of photodetectors (such as photodiodes, photoconductors, photocapacitors or photogates) which generate photo-charges proportional to the radiation (such as light) reflected from an object and received by the

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photosensor. The period of exposure of a photosensor by incident radiation is referred to generally as the integration period. An exposure shutter may control exposure of the photosensor to incident photons. The exposure shutter may be, for example, electrically, mechanically or electro-magnetically operated. The photo-charges are created by photons striking the surface of the solid-state (i.e. semiconductor) material of the photodetectors within the photosensor. As photons strike a photodetector, free charge carriers (i.e., electron-hole pairs) are generated in an amount proportional to the incident photon radiation. The signals from each photodetector may be utilized, for example, to display a corresponding image on a monitor or to provide information about the optical image.

Each photodetector includes a detecting area (also known as the photosensitive area or the detector area) and photodetector circuitry within a common integrated circuit die. The photodetectors receive a portion of the reflected light received at the solid-state imaging device, and collect photo-charges corresponding to the incident radiation intensity falling upon the photodetectors' detecting area of the die. The photo-charges collected by each photodetector are converted to an output analog signal (analog charge signal) or a potential representative of the level of energy reflected from a respective portion of the object. The analog signal (or potential) is then converted to a digital voltage value and processed to create an image.

Solid-state imaging devices are commonly utilized in digital camera devices for both still picture and video applications. In these types of applications, video or still picture quality is related to dynamic range. As result, it is desirable to obtain a digital video or still picture of scenes with a large dynamic range. Despite the differences in CCD, CID and CMOS imager technologies, these technologies typically have the

common problem of limited dynamic range. The dynamic range is defined by the maximum number of photons that a photodetector may collect during a period of photon exposure (also referred to as an integration period) without saturating (i.e., exceeding the capacity of) the photodetector, and the minimum number of photons that
5 a photodetector may collect during the integration period that may be detected over the noise floor. More specifically, the dynamic range is defined as the ratio of the effective maximum detectable signal level (often referred to as "saturation") with respect to the root-mean-square (RMS) noise level of the photosensor.

Solid-state imaging devices that generate photo-charges due to incident photons,
10 such as CCD, CID and CMOS imaging devices, have a dynamic range that is limited by the amount of charge that is collected and held in a given photodetector. As an example, if the saturation of a particular photodetector in a solid-state imaging device is 20,000 electrons, and the incident light on that photodetector is so bright that it creates more electrons than may be held in the photodetector (i.e., greater than 20,000
15 electrons), the excess charge is lost because the excess electrons do not contribute to the signal corresponding to that photodetector. In general, the dynamic range problem is more problematic when the photodetector is an active pixel sensor (APS) cell (i.e., the cell incorporates an active component such as a transistor within the pixel) as compared to a passive pixel sensor (PPS) cell, due to the active components in the APS
20 cells which limit the area available for the detector area, and due to the low voltage supply and clocks utilized in APS cells.

In addition to lost excess charge, excess carriers (i.e., hole-electron pairs) that exceed the amount of charge capable of being stored in the photodetector may cause an undesired blooming phenomenon. Blooming occurs when the excess carriers that

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exceed the saturation level are locally or partially generated, and those excess carriers flow to other photodetectors. In order to avoid blooming, the exposure time of the image may be decreased. However, when the exposure time is lowered, the photodetectors corresponding to the darker portions of the image collect an insufficient amount of charge to provide meaningful information (i.e., the collected charge may be indistinguishable from noise).

Past attempts at solving the limited dynamic range problem have utilized a non-integrating active pixel sensor cell with a non-linear load device, to obtain a logarithmic response. This approach, however, has a number of disadvantages. First, the noise in a non-integrating cell is much higher than the noise in a conventional integrating cell. Also, the exact non-linear transfer function of this type of device is carefully calibrated to avoid variations from cell to cell and compensate for temperature changes. This increases the complexity and inaccuracy of the device.

Another attempt at solving the problem of limited dynamic range was to increase the resolution of the analog-to-digital converters of the solid-state imaging device. However, the higher the precision of an analog-to-digital converters, the slower it operates. This results in a reduced frame rate for a given number of photodetectors and a given number of analog-to-digital converters. Further, as the resolution of an analog-to-digital converter is increased, the least significant bits begin to fill with system noise (including noise from the conversion circuitry itself) rather than meaningful photodetector magnitude information.

Finally, another attempt at solving the limited dynamic range problem utilized a higher supply voltage for the photodetector circuitry so as to increase the charge capacity of each photodetector. A problem with this approach is that the maximum

supply voltage that may be utilized is reduced as semiconductor fabrication processes continue to shrink chip sizes for cost and power advantages.

Thus, a need exists for an improved solid-state imaging device with a substantially increased dynamic range that overcomes the problems and limitations associated with past systems.

SUMMARY

The implementation of a system for improving the dynamic range of solid-state imaging devices may be broadly conceptualized as a solid-state imaging device that comprises an array of photodetectors and additional circuitry that improves dynamic range by accounting for both low illumination and saturation caused by high illumination.

As an example implementation of this system architecture, the solid-state imaging device includes a photosensor for collecting charge created by incident photons, a comparator, and a normalizing circuit. The comparator compares a digital voltage value corresponding to the collected charge, to a predetermined value, and generates a comparison output. The normalizing circuit normalizes the digital voltage value, in response to the comparison output. The solid-state imaging device may also include a memory storage unit that stores normalized voltage values, and a timing control unit that controls the sequencing of photodetectors in the photosensor and the exposure of the photosensor. The invention may also include an indexer for tracking the number of exposure iterations that have occurred.

In another example implementation, the solid-state imaging device performs a method of generating digital images. The method includes collecting a charge in a

photodetector by exposing the photosensor with photons, and comparing the charge to a predetermined value. If the charge is greater than or equal to the predetermined value, the method includes storing a digital voltage value corresponding to the charge. If the charge is less than the predetermined value, the method includes collecting additional charge in the photodetector by re-exposing the photodetector. The method of generating digital images may also include non-destructively reading out the charge stored in the photodetector, normalizing the digital voltage value, and incrementing an index number before re-exposing the photodetector.

Other systems, methods, features and advantages of the invention will be or will become apparent to one with skill in the art upon examination of the following figures and detailed description. It is intended that all such additional systems, methods, features and advantages be included within this description, be within the scope of the invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE FIGURES

The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principals of the invention. Moreover, in the figures, like reference numerals designate corresponding parts throughout the different views.

FIG. 1 is a block diagram illustrating an example implementation of a solid-state imaging device in accordance with the invention.

FIG. 2 is a diagram illustrating a photodetector in the photosensor of FIG. 1.

FIG. 3 is a flow chart illustrating the process performed by the solid-state imaging device of FIG. 1 in generating digital images with improved dynamic range.

FIG. 4 is a flow chart illustrating the process of filling in blank memory locations in the frame memory when "N" is not less than the frame memory width, as shown in FIG. 3.

5 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 illustrates a block diagram of an example implementation of solid-state imaging device 100 in accordance with the invention. The solid-state imaging device 100 includes a photosensor 102, a comparator 104, an indexer 106, a normalizer 108, a frame memory 110, and a timing and control unit 112. For illustration purposes, the photosensor 102 includes a two-dimensional array of photosensitive picture elements ("pixels"), or photodetectors 114. However, it is appreciated by one of ordinary skill in the art that any plurality of photodetectors 114 would satisfy the scope of the invention whether arranged in a one, two or multi-dimensional array topology. Additionally, it is also appreciated that the photosensor 102 may be a complementary metal oxide semiconductor (CMOS) device, charge injection device (CID), charge coupled device (CCD), or other equivalent imaging device. Furthermore, the photodetectors 114 may be active pixel sensor (APS) cell type or passive pixel sensor PPS cell type. All of the photodetectors 114 in the photosensor 102 are substantially similar as the result of the fabrication process utilizing a similar design in the die.

The photodetectors 114, in the photosensor 112, receive incident photon radiation 116 incident on the solid-state imaging device 100 and generate free charge carriers (i.e., electron-hole pairs in an amount proportional to the incident photon radiation 116. The photodetectors 114 receive the incident photon radiation 116, collect photo-charges (referred to as the collected charge) corresponding to the incident photon

radiation 116 intensity and convert the collected photo-charges to an output analog signal (analog charge signal) representative of the level of energy reflected from a respective portion of the object.

The photodetectors 114 are capable of non-destructive read-out of the value of collected charge in each photodetector 114. The non-destructive read-out of the collected charge in each photodetector 114 results in a charge signal 118 corresponding to the collected charge. An analog-to-digital converter "A/D" 120 for converting the charge signal 118 to a digital voltage signal 122 may be built into each photodetector 114, located off the photodetectors 114 (in another part of the die of the solid-state device 100) or located off the solid-state device 100 on a separate device. Alternatively, a separate A/D (not shown) may be included for utilization by all of the photodetectors 114. In either case, the A/D 120 converts the charge signal 118 corresponding to the collected charge from each photodetector 114 to a digital signal (the digital voltage signal 122).

The timing control unit 112 includes an array sequencer 124 with X-Y location outputs 126 and 128 (corresponding to the location of the current photodetector 114) so that each photodetector 114 in the photosensor 102 may be read-out in turn. At each clock pulse, the X-Y location outputs 126 and 128 identify the next photodetector 114, and the collected charge is non-destructively read out. The timing control unit 112 also includes an exposure logic unit 130 that controls the exposures of the photosensor 102. The exposure logic unit 130 receives an index value N 132, and the maximum index signal 134 from the indexer 106. Based on these received signals (132 and 134), the exposure logic unit 130 outputs a exposure control output 136, which controls an exposure shutter (not shown). The exposure shutter may be, for example, a

mechanical, electrical or electro-magnetic shutter. The solid-state imaging device 100 is capable of multiple, cumulative exposures where each of the exposures may be for different lengths of time, as determined by the exposure logic unit 130.

The frame memory 110 stores a normalized voltage value 138 corresponding to each photodetector 114. The frame memory 110 has a storage location corresponding to each photodetector 114 in the photosensor 102. The frame memory 110 may be a random access memory (RAM), read only memory (ROM), non-volatile memory such as flash memory or flash sticks, electrically erasable programmable read only memory (EEPROM), or other equivalent memory devices.

The comparator 104 compares the digital voltage signal 122 corresponding to the stored charge in each photodetector 114 to a predetermined voltage value. The predetermined voltage value is the value corresponding to approximately fifty percent of the maximum charge storage capability of the photodetectors 114. After comparison, the comparator 104 determines whether the storage location in the frame memory 110 (which corresponds to that particular photodetector 114) is blank. A "blank" storage location means that a value of approximately zero is stored in that location. It is appreciated by those skilled in the art that the value of "zero" may actually be slightly greater than zero as a result of noise. The comparator 104 receives information from the frame memory 110 via a data bus 140 between the frame memory 110 and the comparator 104. The comparator 104 may be a standard hardwired comparison logic unit or it may be incorporated into a software controlled microprocessor.

The comparator 104 generates a comparison output 142 based on the comparison of the digital voltage signal 122 to the predetermined voltage value, and

sends this comparison output 142 to a normalizer 108. The normalizer 108 receives both the comparison output 142 from the comparator 104, as well as an index value 144 from the indexer 106. The normalizer 108 is typically a standard hardwired programmable shifter such as, for example, a barrel shifter. However, it is appreciated that the function of the normalizer 108 may be accomplished by a software controlled microprocessor.

The indexer 106 is an incrementing circuit which increments the index value N at the end of each scan of the photosensor 102 by the array sequencer 124 that communicates with the indexer 106 via the timing and control unit 112 through via signal 146. The index value is equal to the number of iterations that have occurred. An iteration includes an exposure and a full scan of the photosensor 102. Thus, for example, after the base exposure and the first scan (i.e., readout) of the photosensor 102, the indexer 106 adds "1" to "0," indicating that one iteration has taken place.

In general, when the comparator 104 determines that (1) the charge stored in a particular photodetector 114 in the photosensor 102 is greater than fifty percent of the maximum charge storage capability of the photodetector 114, and (2) the storage location in the frame memory 110 corresponding to the particular photodetector 114 is blank, then the normalizer 108 receives the comparison output 142 from the comparator 104, instructing the normalizer 108 to shift the digital voltage signal 122 by N bits. Upon receiving the shift instruction via the comparison output 142, the normalizer 108 shifts the digital voltage signal 122 corresponding to that particular photodetector 114 to the right by a number of bits equal to N, where N is equal to the current index number as indicated by the index output 144. The index output 144 is determined by the indexer 106, which may be a standard hardwired incrementing logic circuit or

incorporated into a software controlled microprocessor. The indexer 106 increments the index value by one after the array sequencer 124 completes a full scan of the photosensor 102.

If the comparator 104 determines that either the charge stored in a photodetector 114 in the photosensor 102 is not greater than fifty percent of the maximum charge storage capability of the photodetector 114, or the storage location in the frame memory 110 corresponding to the particular photodetector 114 is not blank, the normalizer 108 receives the comparison output 142 from the comparator 104, instructing the normalizer 108 not to shift the digital voltage signal 122. After receiving a "no-shift" instruction via the comparison output 142, the normalizer 108 ignores the corresponding digital voltage signal 122, and nothing is stored in the frame memory 110.

In FIG. 2, a photodetector 114, FIG. 1, is shown. The photodetector 114 includes a detecting area 200, FIG. 2, (also known as the photosensitive area or the detector area) and photodetector circuitry 202. The detecting area 200 is the portion of the photodetector 114 that receives photon radiation 116 incident upon the solid-state imaging device 100, FIG. 1, and converts the received photon radiation 116 into photo-charges via free charge carriers. The photodetector circuitry 202 converts the photo-charges into an output analog signal (analog charge signal) or potential representative of the level of energy reflected from a respective portion of an object. The photodetector circuitry 202 may also include active circuitry such as a transistor and an A/D converter.

FIG. 3 illustrates an example process performed by the solid-state imaging device 100 in FIG. 1. The process begins in step 300, FIG. 3, by initializing the solid-state

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collected charge in the photodetector 114, FIG. 1, so that subsequent exposures will result in a cumulative collection of charge. The non-destructive read-out includes an A/D conversion step (not shown). Each photodetector 114 may include an embedded A/D 120 for converting the charge signal 118 to a digital voltage signal 122 or the A/D 120 may be located off the photodetectors 114 (in another part of the die of the solid-state device 100) or located off the solid-state device 100 on a separate device. Alternatively, a separate A/D (not shown) may be included for utilization by all of the photodetectors 114. In either case, the A/D 120 converts the charge signal 118 corresponding to the collected charge from each photodetector 114 to the digital voltage signal 122. The digital voltage signal 122 corresponding to the amount of charge collected in the photodetector 114 is sent to the comparator 104 for comparison in step 310, FIG. 3.

During the decision step 310, the comparator 104, FIG. 1, determines whether the digital voltage signal 122 corresponding to the amount of charge collected in the photodetector 114 currently being analyzed or read-out (" V_{pixel} "), is greater than a predetermined voltage value (" V_{pre} "), and whether the frame memory 110 storage location corresponding to the photodetector 114 currently being analyzed or read-out is blank. As an example, the photodetector 114 currently being analyzed or read-out is referred to as the current pixel. If both of these conditions are satisfied (i.e., $V_{\text{pixel}} > V_{\text{pre}}$; and the memory location corresponding to the current pixel is blank), then, the normalizer 108 normalizes the digital voltage signal 122, and outputs a normalized voltage value 138 to the frame memory 110 in step 312, FIG. 3.

In step 312, if the normalizer 108, FIG. 1, is a shifter, the normalizer 108 shifts the digital voltage signal 122, V_{pixel} , to the right by N bits, where "N" is the current

index value. As an example, typically during the base exposure $N=0$. Thus, the digital voltage signal 122 corresponding to any photodetectors 114 which meet both conditions (i.e., $V_{\text{pixel}} > V_{\text{pre}}$; and the memory location corresponding to the current pixel is blank) after the base exposure, will be shifted zero bits by the normalizer 108.

5 The normalized voltage value 138 is then stored in a corresponding location in the frame memory 110 in step 314, FIG. 3. Once the digital voltage signal 122, FIG. 1, for the current pixel is stored in the frame memory 110 in step 314, FIG. 3, the X-Y location outputs 126, FIG. 1, and 128 of the timing control unit 112 proceed to the next photodetector 114 in the photosensor 102, in step 318, FIG. 3. As an example, if the
10 previously read photodetector 114, FIG. 1, was at (3,5), the X-Y location outputs 126 and 128 may proceed to the photodetector 114 at (3,6). However, if the previously read photodetector 114 was the last one in the photosensor 102 (i.e., (m, n) in a photosensor 102 with “m” columns and “n” rows) in step 316, FIG. 3, then a full iteration has been completed. The indexer 106, FIG. 1, receives a signal indicating that the scanning of
15 the photosensor 102 by the timing control unit 112 has started over (i.e., the X-Y location outputs 126 and 128 have returned back to (1,1)) in step 320, FIG. 3.

The solid-state imaging device 100, FIG. 1, next determines whether the current index value “N” is less than the frame memory width “W” in step 322, FIG. 3. The frame width W is the number of bits in each memory location of the frame memory
20 110. The indexer 106 compares the current index value N with the frame memory 110 width W to determine whether the current index value N is less than the frame memory 110 width W. The indexer 106 then sends the current index value N, via signal 132, to the timing control unit 112 and the “maximum index” signal 134 to the comparator 104. If the maximum index signal 134 indicates that the current index value N (signal 132)

is not less than the frame memory 110 width W, then no additional exposures take place, and all of the blank memory locations in the frame memory 110 are filled in step 326, FIG. 3. The process then ends in step 328. It is appreciated that the current index value N may be also compared to a predetermined value other than the frame memory 100, FIG. 1, width without effecting the spirit of the invention.

If the current index value N 132 is less than the frame memory width W, then the indexer 106 increments the index value N, which indicates a new iteration, and the index value is incremental in step 324, FIG. 3. The photosensor 102 is then exposed again in step 306. The new exposure is for a period of time so that the total exposure time is equal to $x \cdot 2^N$, where "x" is the base exposure period, and "N" is the index value (i.e., the number of iterations that have occurred). As an example, if $N=0$, the total exposure time is equal to "x".

As a result, the new net exposure will be equal to the total exposure time ($x \cdot 2^N$) minus the total exposure time from the previous iteration. As an example, if "x," the base exposure time, is equal to 10mS, the exposure times for each iteration are described in Table 1:

Iteration = Index = N	Total exposure = $x \cdot 2^N$	New exposure = $(x \cdot 2^N) - (\text{previous exposure})$
0	10mS	$(10 - 0) = 10\text{mS}$
1	20mS	$(20 - 10) = 10\text{mS}$
2	40mS	$(40 - 20) = 20\text{mS}$
3	80mS	$(80 - 40) = 40\text{mS}$
4	160mS	$(160 - 80) = 80\text{mS}$
5	320mS	$(320 - 160) = 160\text{mS}$
6	640mS	$(640 - 320) = 320\text{mS}$

Table 1

After the new exposure of step 306, steps 308, 310, 312 and 314 are repeated. That is, the photodetectors 114 are again non-destructively read-out in turn in step 308, the decision step 310 is repeated, and, if the comparison indicates it is appropriate, the digital voltage signals 122 are shifted and stored in steps 312 and 314. However, if, at the decision step 310 the comparator 104 determines that for the current pixel, either V_{pixel} is not greater than V_{pre} or the memory location corresponding to the current pixel is not blank, then the shifting and storage steps 312 and 314 are skipped for the current photodetector 114 during the current iteration, and the timing control unit 112 moves on to the next photodetector 114.

FIG. 4 is a flow chart illustrating the filling in of the blank memory locations in the frame memory when "N" is not less than the frame memory 110, FIG. 1, width, as described in step 326 of FIG. 3. The process begins in step 400. When the indexer 106, FIG. 1, determines that the current index value N is not less than the frame memory 110 width in step 322, FIG. 3, the indexer 106, FIG. 1, sends the "maximum index" signal 134 to the comparator 104 indicating that the current index value N is not less than the frame memory 100 width W in step 402, FIG. 4. This maximum index

signal 134, FIG. 1, prevents any additional exposures from occurring, and overrides the comparison of V_{pixel} and V_{pre} by the comparator 104. As an example, this may be done by a switch ("fill-in switch") in the comparator 104 that, when switched on, always generates a comparison output 142 instructing the normalizer 108 to shift the digital voltage signal 122. Upon receiving the "maximum index" signal 134 from the indexer 106, the fill-in switch is switched on, and the comparator 104 sends the normalizer 108 a constant shift message, even if V_{pixel} is less than V_{pre} .

Then, the first photodetector 114 is non-destructively read out in step 404, FIG. 4, and the comparator 104, FIG. 1, determines if the corresponding location in the frame memory 110 is blank in decision step 406, FIG. 4. If the location in the frame memory 110, FIG. 1, is blank, the normalizer 108 shifts the corresponding digital voltage signal 122 to the right by "N" bits in step 408, FIG. 4, and the normalized voltage value 138, FIG. 1, is stored in the appropriate location in the frame memory 110 in step 410, FIG. 4. Then, the timing control unit 112, FIG. 1, sequences to the next photodetector 114. If the frame memory 110 location is not blank, then the shifting and storing steps 408, FIG. 4, and 410 are skipped, and the timing control unit 112, FIG. 1, sequences to the next photodetector 114 in step 412, FIG. 4. The "filling in" process of step 326 continues throughout the photosensor 102, FIG. 1, until the photosensor 102 is completely scanned. When the photosensor 102 is completely scanned (i.e., the last photodetector 114 in the photosensor 102 has been reached, step 414, FIG. 4), the fill-in process is finished and the image generation is complete in step 328.

While various embodiments of the application have been described, it will be apparent to those of ordinary skill in the art that many more embodiments and

implementations are possible that are within the scope of this invention. Accordingly, the invention is not to be restricted except in light of the attached claims and their equivalents.

What is claimed:

1. A solid-state imaging device comprising:

a photosensor for collecting charge created by incident photons; and

a comparator for comparing a digital voltage value corresponding to the
5 collected charge, to a predetermined value, and generating a compare output.
2. The solid-state imaging device of Claim 1 further including a
normalizing circuit for normalizing the digital voltage value, in response to the
comparison output, and outputting a normalized voltage value.
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3. The solid-state imaging device of Claim 1 wherein the photosensor is an
array of photodetectors.
4. The solid-state imaging device of Claim 3 wherein the photodetectors
15 are CMOS devices.
5. The solid-state imaging device of Claim 3 further including at least one
digital voltage value corresponding to the charge stored in each photodetector.

6. The solid-state imaging device of Claim 5 further including a frame memory for storing the normalized voltage values.

7. The solid-state imaging device of Claim 6 further including a timing control unit for controlling sequencing of the photodetectors.

8. The solid-state imaging device of Claim 7 wherein the timing control unit includes an array sequencer and an exposure logic unit.

9. The solid-state imaging device of Claim 8 further including an indexer for providing an index number to the normalizing circuit.

10. The solid-state imaging device of Claim 9 further comprising a data bus for transferring data between the frame memory and the comparator.

11. The solid-state imaging device of Claim 10 wherein the normalizing circuit is a programmable shifter.

12. The solid-state imaging device of Claim 11 wherein the programmable shifter shifts the digital voltage values by a predetermined number of bits.

13. The solid-state imaging device of Claim 12 wherein the predetermined
5 number of bits is equal to the index number.

14. The solid-state imaging device of Claim 13 wherein the normalizing unit is a barrel shifter.

10 15. The solid-state imaging device of Claim 7 wherein the timing control unit comprises a first output corresponding to a row-number of the array of photodetectors, and a second output corresponding to a column-number of the array of photodetectors.

15 16. A method of generating digital images having improved dynamic range comprising:

collecting a charge in a photodetector by exposing the photodetector with photons for a first predetermined period of time;

comparing the charge to a predetermined value;

if the charge is greater than or equal to the predetermined value, storing a digital voltage value corresponding to the charge; and

if the charge is less than the predetermined value, collecting additional charge in the photodetector by re-exposing the photodetector for a new period of time.

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17. The method of claim 16 further including non-destructively reading the charge.

18. The method of claim 17 further including normalizing the digital voltage
10 value to generate a normalized voltage value.

19. The method of claim 18 wherein the step of storing comprises storing the normalized digital value.

15 20. The method of claim 19 wherein the step of storing further comprises storing the normalized voltage value in a location in a frame memory.

21. The method of claim 20 further including clearing the location in the frame memory before collecting the charge.

22. The method of claim 21 wherein the step of storing the normalized voltage value in the location in the frame memory comprises storing the normalized voltage value in the location in the frame memory only if the location in the frame memory is blank.

23. The method of claim 22 further including incrementing an index number before collecting additional charge in the photodetector.

24. The method of claim 23 wherein the normalizing step comprises shifting the digital voltage value to the right by a predetermined number of bits.

25. The method of claim 24 wherein the normalizing step comprises shifting the digital voltage value to the right by a number of bits equal to the index number.

26. The method of claim 25 further including storing the normalized voltage value, if the charge is less than the predetermined value, and if the index number is greater than a predetermined index value.

27. The method of claim 25 further including storing the normalized voltage value, if the charge is less than the predetermined value, and if the index number is greater than a width of the location in the frame memory.

28. The method of claim 19 wherein the step of collecting additional charge comprises re-exposing the photodetector with photons for a period of time equal to

$$x \cdot 2^{(N-1)}$$

where x is equal to the first predetermined period of time and N is equal to the index number.

29. A solid-state imaging device comprising:

means for collecting charge created by incident photons; and

means for comparing a digital voltage value corresponding to the collected charge, to a predetermined value, and generating a comparison output.

30. The solid-state imaging device of Claim 29 further including a means for normalizing the digital voltage value, in response to the comparison output, and outputting a normalized voltage value.

31. The solid-state imaging device of Claim 29 wherein the collecting means is an array of photodetectors.

32. The solid-state imaging device of Claim 31 wherein the photodetectors
5 are CMOS devices.

33. A system for generating digital images having improved dynamic range comprising:

- means for collecting a charge in a photodetector by exposing the photodetector
10 with photons for a first predetermined period of time;
- means for comparing the charge to a predetermined value;
- means for storing a digital voltage value corresponding to the charge if the charge is greater than or equal to the predetermined value; and
- 15 means for collecting additional charge in the photodetector by re-exposing the photodetector for a new period of time if the charge is less than the predetermined value.

34. The system of claim 33 further including means for non-destructively reading the charge.

35. The method of claim 34 further including means for normalizing the digital voltage value to generate a normalized voltage value.

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ABSTRACT

The disclosure is a solid-state imaging device, including a photosensor for collecting charge created by incident photons, a comparator for comparing a digital voltage value corresponding to the collected charge, to a predetermined value, and generating a comparison output, and a normalizing circuit for normalizing the digital voltage value, in response to the comparison output.

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Solid-state Imaging Device 100

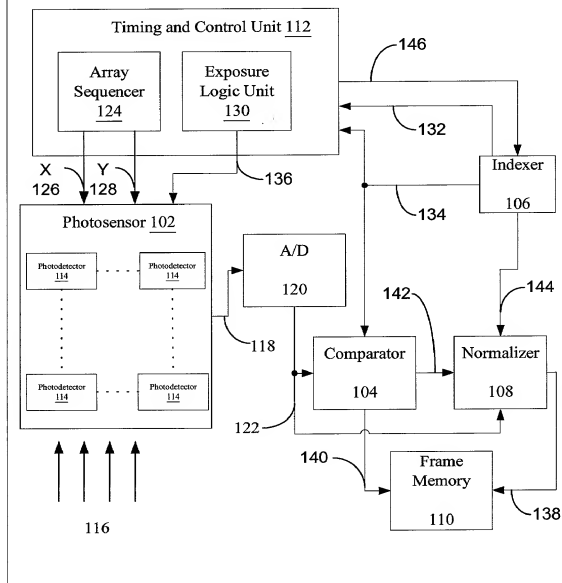


FIG. 1

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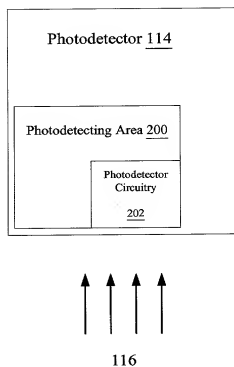


FIG. 2

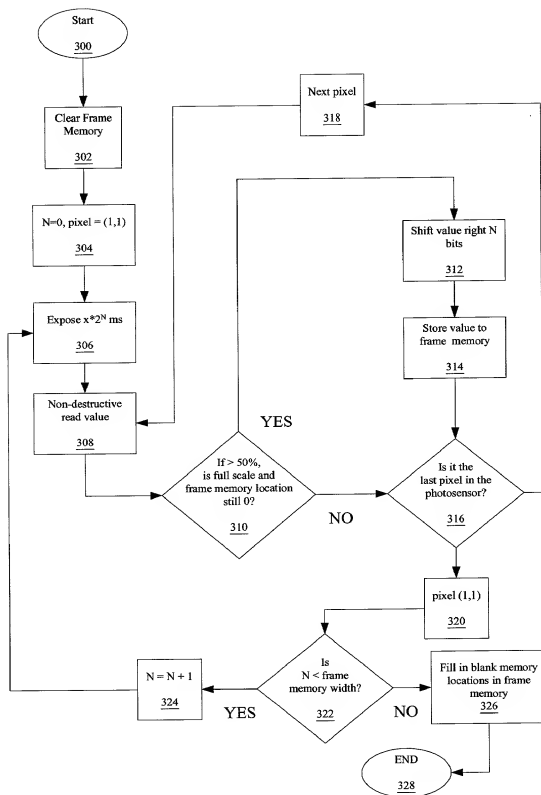


FIG. 3


```
graph TD
    322[From 322] --> 400([Start 400])
    400 --> 402[Send "maximum index" signal to comparator 402]
    402 --> 404[Non-destructive read value 404]
    404 --> 406{Is frame memory location still 0? 406}
    406 -- YES --> 408[Shift value right N bits 408]
    408 --> 410[Store value to frame memory 410]
    410 --> 414{Is it the last pixel in the photosensor 414}
    414 -- YES --> 328([END 328])
    414 -- NO --> 412[Next pixel 412]
    406 -- NO --> 412
    412 --> 404
```

FIG. 4

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare:

That my residence, post office address and citizenship are as stated below next to my name.

That I verily believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

the specification of which (check one)

(X) is attached hereto.

() was filed on _____ as

Application Serial No. _____

and was amended on _____

That I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

That I acknowledge the duty to disclose information known to be material to patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

That I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)
Claimed

Priority

☐
(Number)

(Country)

(Day/Month/Year Filed)

:

☐
(Number)
No

(Country)

(Day/Month/Year Filed)

:

Yes

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

(Application Number)

(Filing Date)

(Application Number)

(Filing Date)

That I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

United States Application(s)

(Application Serial No.)
abandoned)

(Filing Date)

(Status)-(Patented, pending,

(Application Serial No.)
abandoned)

(Filing Date)

(Status)-(Patented, pending,

That all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

I hereby appoint the following attorneys, with full power of substitution and revocation, to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith and request that all correspondence and telephone calls in respect to this application be directed to **Francisco A. Rubio-Campos at SONNENSCHN, NATH & ROSENTHAL, P. O. Box 061080; Wacker Drive Station, Sears Tower, Chicago, Illinois 60606-1080.**

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